SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

THERMAL CHARACTERISTICS OF THE PENTAWATT-HEPTAWATT PACKAGES

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INTRODUCTION

This Application Note is aimed to give a complete thermal characterization of the Heptawatt and Pentawatt package (fig. 1, 2).

Characterization is performed according with recomendations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repeated pulses, with different pulse width and duty cycle ;
4. thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Pentawatt.

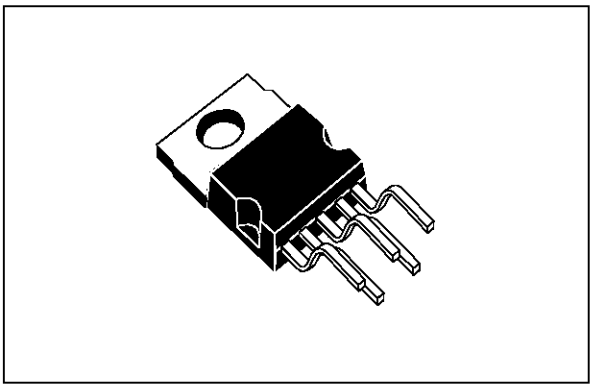
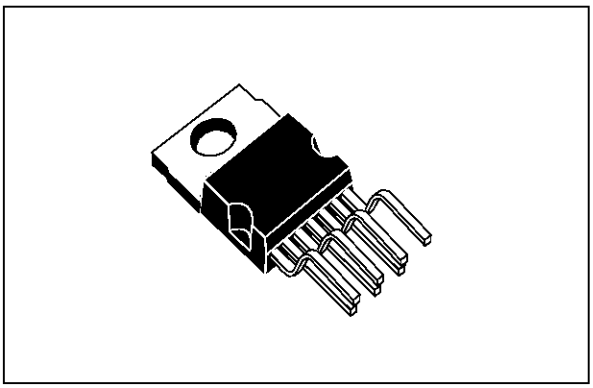


Figure 2 : Heptawatt.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 15k mils^2 die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2k mils^2 with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package	Pentawatt - Heptawatt
Frame Material	Copper
Slug Thickness	1.25mm Typ.
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 3. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady state $R_{th(j-a)}$ can be found, according with pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 (Thermalloy) whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all of the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 4. The absolute value and the behaviour with the dissipated power are the same for

both packages as the slug thickness and the die - attach are equal.

Figure 3 : Measurement of $R_{th\ (j-c)}$.

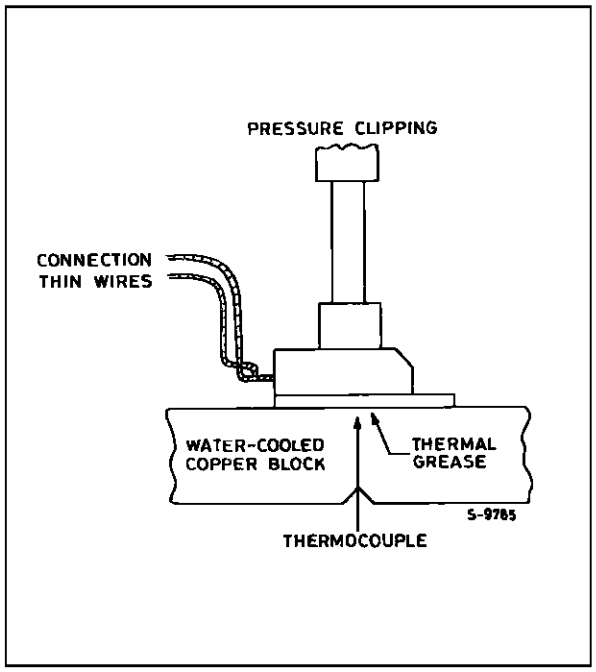
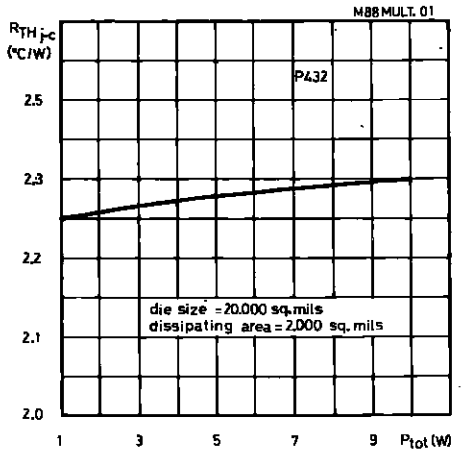


Figure 4 : $R_{th\ (j-c)}$ of Pentawatt and Heptawatt Package vs. Power Level.

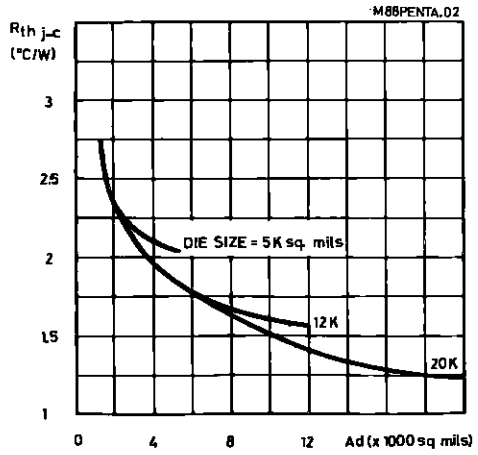


It is well known that the main contribution to $R_{th(j-c)}$ of power packages is given by the silicon die.

FOR OTHER DEVICES THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 5 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 5 : $R_{th\ (j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power application (1W), the Pentawatt and Heptawatt packages can be used without external heat sink thanks to the significant size (about 1.5cm^2) of its integrated thermal mass.

An effective cost solution for higher power application (1.5-2.0W) is using a copper area heat sink.

An board with the external leads bent down as shown in fig. 7.

Fig. 6 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern in still air, on PC board, on integrated heat sink on board and on a commercial heat sink.

IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 6 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 5 CORRECTION TERM IS ALWAYS IN THE RANGE OF 0-2°C/W ; THEREFORE, IT AFFECTS THE $Rth_{(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED IN PC BOARD.

Figure 6 : $R_{th\ (j\text{-}a)}$ vs. dissipated Power (heptawatt).

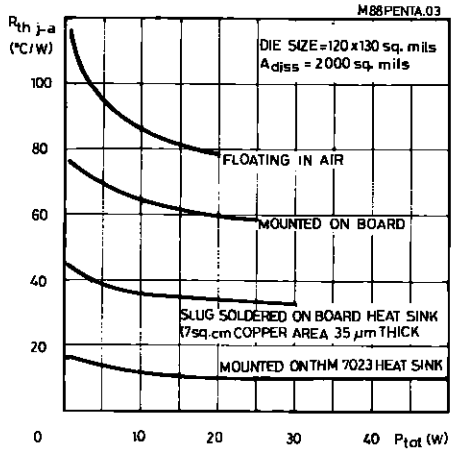
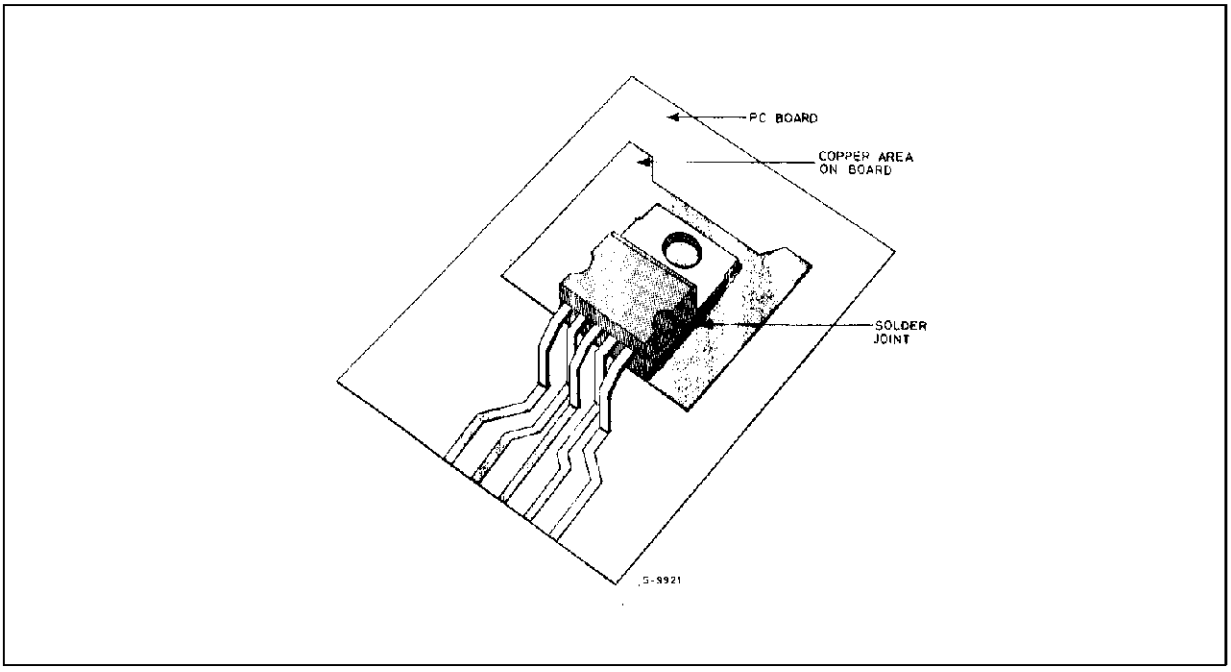


Figure 7 : Pentawatt Soldered on Copper Heatsink on P.C Board.

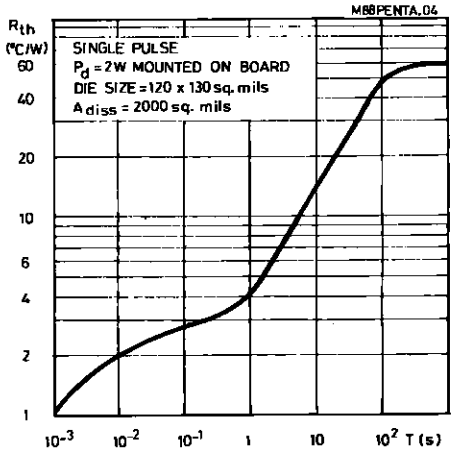


TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height without any external heat sink is shown in fig. 8.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance (C = 1J/°C) and a correspondingly long risetime (τ = 80s), single pulses up to 20W can be delivered for 1 s with acceptable junction temperature increase.

Figure 8 : Transient Thermal Resistance for Single Pulses (heptawatt).

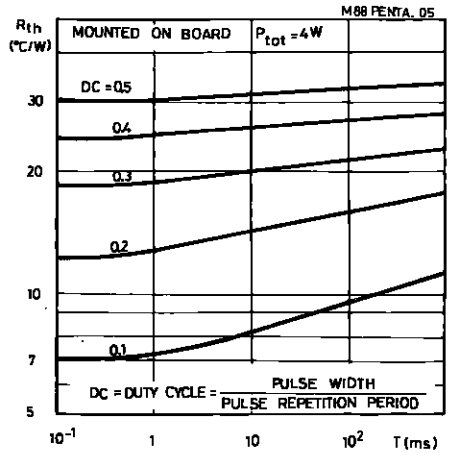


IN ORDER TO HAVE ACCURATE $R_{th}(t_o)$ FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Repetition of pulses with defined Pd, period and duty cycle DC (ratio between pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 9 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

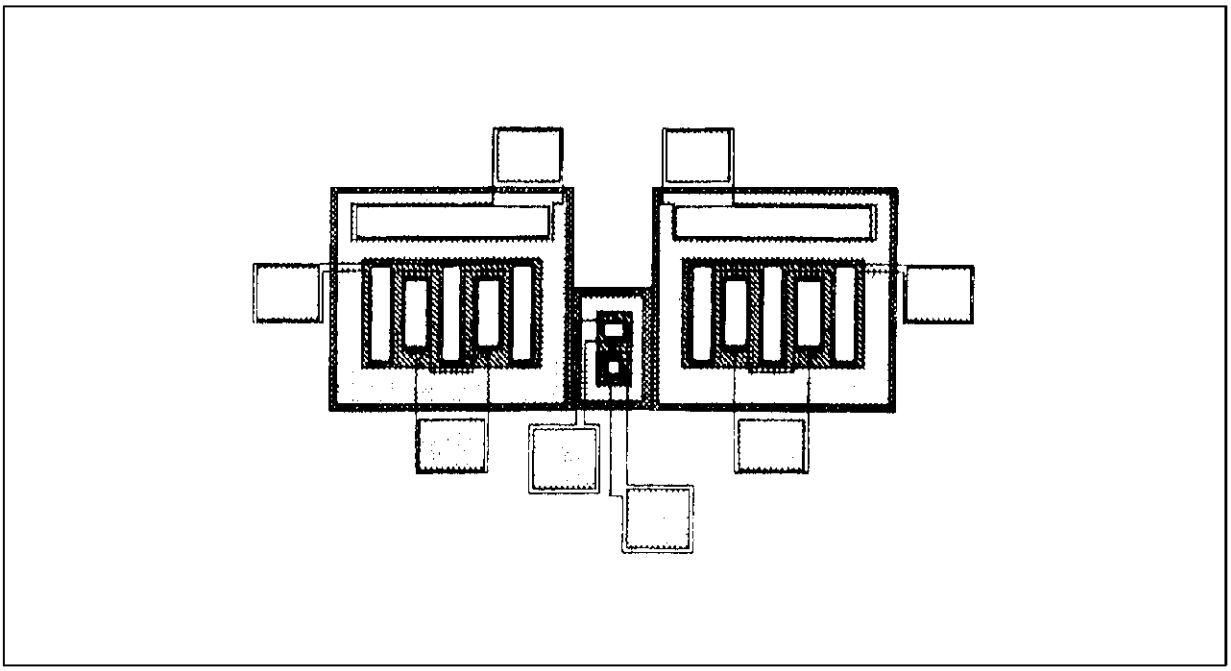
Figure 9 : Peak Transient R_{th} vs Pulse width and Duty Cycle (heptawatt).



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sending diode (fig. A1). The active area is about 2000 $mils^2$ on a 15000 $mils^2$ chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

Figure A1 : Test Pattern P432 Lay-out.



The relationship between the forward voltage V_f of the diode at a constant current of 100µA and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A2 : Calibration Curve (sensing diode).

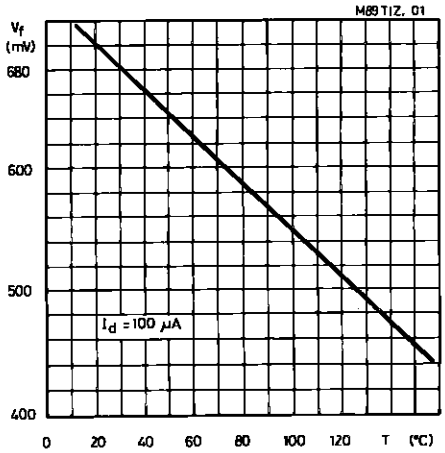
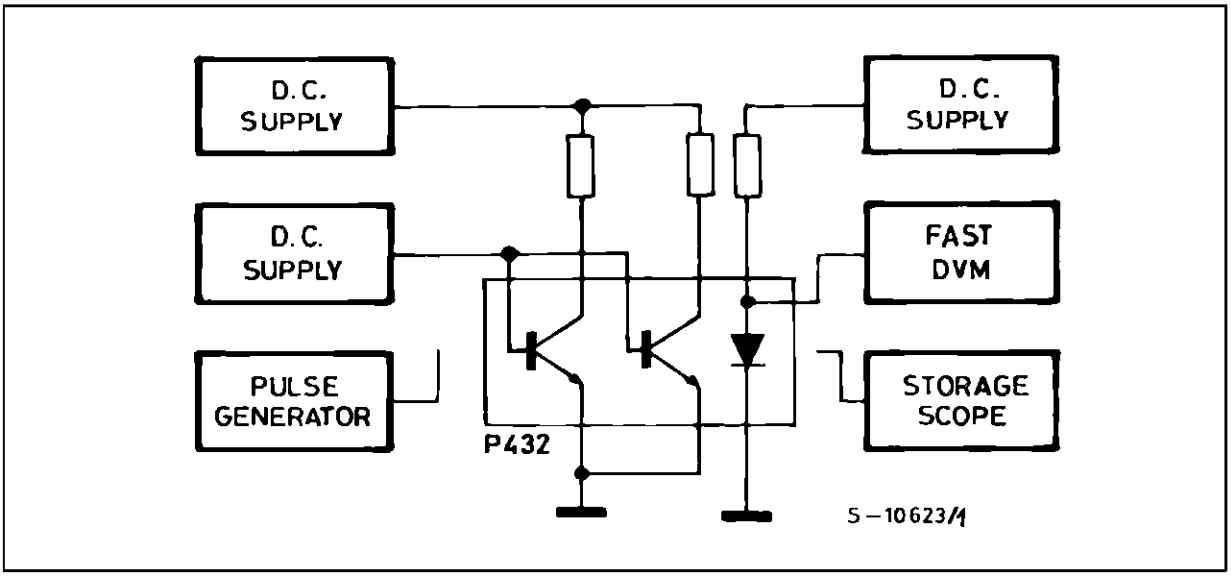


Figure A3 : Measurement Circuit.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

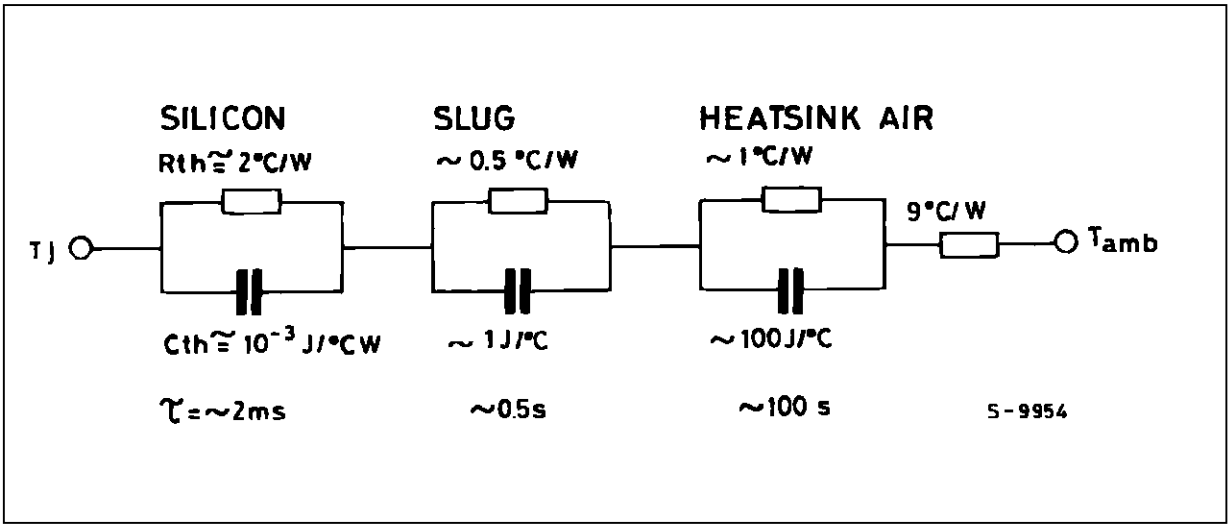
The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink Rth can be calculated from the relationship :

$$R_{th} = \frac{1}{K \times S}$$

Where K is the thermal conductivity of the material, 1 the length of the conductive path and S its section.

Figure B1 : Electrical Equivalent of Pentawatt and Heptawatt Package mounted on the External Heatsink.



Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Each cell has its own risetime τ, given by the product of thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

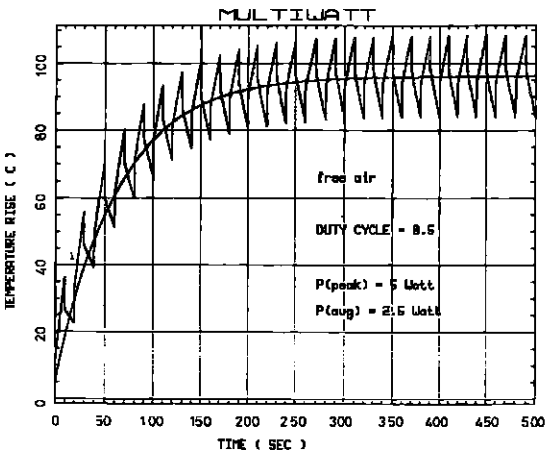
The value of the time constant determines whether a cell approaches equilibrium rapidly or slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d \times [1 - e^{-t/\tau}] \quad (1)$$

Typical values of R_{th}, C_{th} and τ for Heptawatt and Pentawatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitance while the value reached in the steady state depends on thermal resistance only. Qualitative beahaviour of the network of fig. B1 is shown in fig. B2.

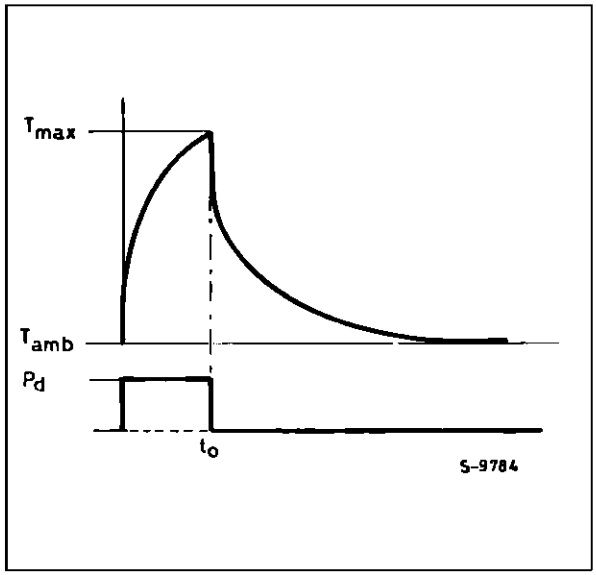
Figure B2 : Qualittative T_j increase (network of fig. B1) for repeated power pulse (heptawatt).



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_o, a transient thermal resis-tance R_{th} (t_o) is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorter pulses, R_{th} (t_o) is lower and a higher power can be dissipated, without exceeding the maximum junction temperature $T_{j\,max}$ allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of R_{th} (t_o) for the two cases of the Heptawatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height Pd are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = Pd \times DC$$

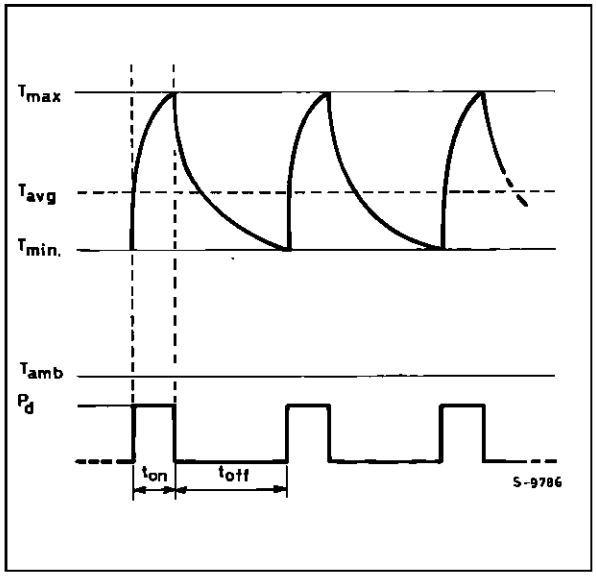
The average temperature increase is :

$$\Delta T_{avg} = R_{th} \times Pd_{avg} = R_{th} \times Pd \times DC$$

On the other hand, the silicon die ($\tau_{SI} = 1 \div 2$ms) is able to follow frequencies of some kHz and junction temperature oscillates about the average, as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resis-tance $R_{th\,peak}$) is now given by fig. 5, and can be obtained if pulse length and duty cycle are known ; Pd_{max} is derived from the same figure.

Figure B4 : Junction Temperature increase for operated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM Pd FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum Pd for a single pulse with a length of 20ms in the case of Heptawatt package used without heat sink. Ambient temperature is 50°C ; maximum temperature is 130°C. Die size is 15k mils^2, with dissipating area of 2k mils^2 (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is 80°C. Having a $R_{th(j-a)}$ of 60°C/W, Heptawatt package can dissipate about 1.3W in steady state From fig. 8 the transient thermal resistance corresponding to one single pulse of 20ms in R_{th} $(20ms)_{P432}$ = 2.2°C/W. A peak of 80/2.2 = 36.3W can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area.

Pratical case : IC having a die size of 15k mils^2 with a dissipating area of 10k mils^2.

SOLUTION : from fig. 5, thermal resistance of P432 and of the IC under consideration are $R_{th\,P432}$ = 2.3°C/W and $R_{th(j-c)IC}$ = 1.5°C/W.

As the length of the pulse is 10-15 times longer than the risetime of the silicon, the die (first cell of fig. B1)

can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$.

$$R_{th}\ (20ms)_{IC} = R_{th}\ (20ms)_{P432} - R_{th(j-c)P432} + R_{th(j-c)IC} =$$
$$= 2.2 - 2.3 + 1.5°C/W = 1.4°C/W$$

A single pulse of 80/1.4 ≡ 57W can be delivered to such a device.

EXAMPLE 3 - CORRECTION FOR SINGLE PULSES OF 1–3ms

PROBLEM : Correct the results of example 2, for pulse length of 1ms.

SOLUTION : when the pulse has the same order of magnitude of silicon rise time (τ_{P432} is about 1ms) another type of correction is needed. In first approximation it is considered that remains constant when the dissipating area gets higher and the Rth for the silicon die decreases as the reciprocal of the dissipating area. From relationship (1) :

$\Delta T = R_{th}\ (1ms)_{P432} \times 2K/10K \times Pd \times [1 - e^{-t/\tau}]$ for t_o = 1ms :

$$R_{thIC}\ (1ms) = 1.05/0.5°C/W \equiv 0.21°C/W$$

A single pulse of 80/0.21 ≡ 380W can be delivered to such a device.

EXAMPLE 4 - Rth REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Heptawatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is 50°C. maximum temperature is allowed to be 125°C.

SOLUTION : a maximum ΔT = 75°C has to be considered. Fig. 9 indicated that for a pulse width of 10ms and a duty cycle of 0.1, Rth_{peak} is 8.5°C/W. Maximum Pd is 75/8.5 = 8.8W, with an average temperature increase ΔT_{peak} of 60 x 0.1 x 8.8 ≡ 68°C.

REFERENCES

"Improved thermal evaluation, by means of a simple integrated structure" T. Hopkins, C. Cognetti, R. Tiziani - SEMI THERM (USA, 1986).